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(54) **METHOD OF MAKING FLOATING-GATE MEMORY-CELL ARRAY WITH DIGITAL LOGIC TRANSISTORS**

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(57) **ABSTRACT**

A nonvolatile memory array is encased in a P-well, and the P-well encased in a deep N-well, the two wells separating the memory array from the integrated circuit substrate and from the other circuitry of the integrated circuit. At the same time the deep N-well is formed for the nonvolatile memory array, deep N-wells are formed for the high-voltage P-channel transistors of the logic circuitry. At the same time the P-well is formed for the nonvolatile memory array, P-wells are formed for the low-voltage N-channel transistors. The memory array contains nonvolatile cells of the type used in ultra-violet-erasable EPROMs. During erasure, the isolated-well formation allows the source, the drain and the channel of selected cells to be driven to a positive voltage. The isolated well is also driven to a positive voltage equal to, or slightly greater than, the positive voltage applied to the source and drain, thus eliminating the field-plate breakdown-voltage problem.

10 Claims, 5 Drawing Sheets